

TD: DIRECTIONS IN COMPUTING AND SIGNALING

Session Chair: Ali Keshavarzi, TSMC, San Jose, CA
Associate Chair: Satoshi Shigematsu, NTT, Atsugi, Japan

28.1 Optical I/O Technology in Tera-Scale Computing**1:30 PM**

I. Young, E. Mohammed, J. Liao, A. Kern, S. Palermo, B. Block, M. Reshotko, P. Chang
Intel, Hillsboro, OR

An optical I/O architecture with 90nm CMOS circuits, 1×12 VCSEL/detector arrays and polymer waveguides achieves packaged 10Gb/s/channel at 11pJ/b, while a pre-emphasis TX enables potential 18Gb/s at 9.6pJ/b link efficiency. Increased optical CMOS I/O integration with ring resonator modulators and Ge detectors projects to near 1pJ/b with current 20Gb/s performance.

28.2 Wireless DC Voltage Transmission Using Inductive-Coupling Channel for Highly-Parallel Wafer-Level Testing**2:00 PM**

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An inductive-coupling DC-voltage transceiver realizes a low-cost, highly-parallel screening test on wafer. It can output a DC voltage with 6b resolution without any area-consuming digital or synchronization circuits, and corrects the output voltage error without needing calibration circuits on the die-under-test. All the circuits for DC tests are implemented into the area of a 100×100μm² inductor.

28.3 A Stretchable EMI Measurement Sheet with 8×8 Coil Array, 2V Organic CMOS Decoder, and -70dBm EMI Detection Circuits in 0.18μm CMOS**2:30 PM**

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A stretchable 12×12cm² EMI measurement sheet is developed to enable the measurement of the EMI distribution on the surface of the electronic devices by wrapping the devices in the sheet. The sheet includes 8×8 coil array, 2V organic CMOS decoder, 40% stretchable interconnects with carbon nanotubes, and -70dBm EMI detection circuits in 0.18μm CMOS.

Break 3:00 PM

28.4 Field-Coupled Nanomagnets for Interconnect-Free Nonvolatile Computing**3:15 PM***M. Becherer¹, G. Csaba¹, R. Emling¹, W. Porod², P. Lugli¹, D. Schmitt-Landsiedel¹*¹Technical University Munich, Munich, Germany²University of Notre Dame, South Bend, IN

This paper presents the potential of programmable ferromagnetic computing devices composed of thin focused ion beam patterned Co/Pt films with 2.2×10^9 devices/cm² and nonvolatile behavior. They offer rad-hard and parallel information processing at 300K and can be accessed by electrical input and output. These logic devices offer $\sim 5 \times 10^{-18}$ J energy per switching event and overcome the shortcomings of electrical wiring by a contactless clocking scheme.

28.5 Chip-Scale Camera Module (CSCM) Using Through-Silicon-Via (TSV)**3:45 PM***H. Yoshikawa, A. Kawasaki, T. Iizuka, Y. Nishimura, K. Tanida, K. Akiyama, M. Sekiguchi, M. Matsuo, S. Fukuchi, K. Takahashi*

Toshiba Semiconductor, Yokohama, Japan

TSV technology is applied to a CMOS image sensor module and a size reduction of 55% in volume and 36% in footprint is achieved. Optimization of TSV parasitic circuits achieves electrical performance comparable with the conventional product that uses bonding wires. The saving of passive components and their related assembly allows a cost reduction of 25% when employing TSV technology.

28.6 A Subjective-Contour Generation LSI System with Expandable Pixel-Parallel Architecture for Vision Systems**4:15 PM***T. Morie, Y. Kim*

Kyushu Institute of Technology, Kitakyushu, Japan

A 0.25 μ m CMOS LSI containing 35 \times 35pixel units executes a directional (anisotropic) diffusion algorithm that consists of a simple cellular-neural-network-based updating rule, and generates analog ridge-like diffusion states by propagating the internal state of pixel units in the given direction. Experimental results are shown for subjective contour generation.

28.7 An Inductive-Coupling Link for 3D Integration of a 90nm CMOS Processor and a 65nm CMOS SRAM**4:45 PM***K. Niitsu¹, Y. Shimazaki^{1,2}, Y. Sugimori¹, Y. Kohama¹, K. Kasuga¹, I. Nonomura², M. Saen³, S. Komatsu³, K. Osada³, N. Irie³, T. Hattori², A. Hasegawa², T. Kuroda¹*¹Keio University, Yokohama, Japan²Renesas Technology, Tokyo, Japan³Hitachi, Tokyo, Japan

A 90nm CMOS 8-core processor is mounted face down on a package by C4 bump and a 65nm CMOS 1MB SRAM is glued on it face up. The two chips operating with different supply voltages are AC-coupled by inductive coupling that provides 19.2Gb/s data link. Measured power and area efficiency of the link is 1pJ/b and 0.15mm²/Gb/s, which is 1/30 and 1/3 in comparison with the DDR2 interface, respectively.

Conclusion**5:00 PM**